Testing Intersil's "Active Filter Designer" Gain and Q Sequencing Impact on Output Noise

Introduction

Intersil's Active Filter Designer is a simulation suite intended to accelerate a designer's progress towards a working active filter implementation by assisting in the op amp selection and component value solutions. It can quickly generate and verify a multi-stage design online through gain and phase simulation, step transient simulation, and noise analysis. In addition, the tool allows users to download the schematic for use in our iSim: PE simulation software, where further simulation or analysis can be accomplished.

The filter tool is intended to support LowPass (LP), HighPass (HP), and Bandpass (BP) filter requirements. The tool presently supports LowPass filter design with HP and BP intended for addition to the tool in 2010. For a more in depth look at the "Active Filter Designer" please reference AN1548 [1].

The tool will default to a semi-automatic design flow where it will assign the gains and sequence the Q's using a built in algorithm. Manual stage targets can also be entered to override these selections. One of the more common queries in the Intersil tool is the way the gain and quality factor (Q) are sequenced for filter designs with an order >2 and total gain >1. The tool sequences the poles from high Q to low Q in ascending gains, for example a 4th order Butterworth filter will have the first stage with the lowest gain but the highest Q while its 2nd stage will contain the most gain and the lower Q. This is contrary to what is commonly seen in the industry and academia. In [2] we find that, if gain is required in the filter, then it should come in the early stages to reduce noise at the output. That reference also mentions that arranging the stages in order of increasing Q is an excellent guideline to avoid saturation or clipping in the op amps.

This application note will show through simulation that Intersil's gain partitioning algorithm and Q sequencing can deliver improved integrated noise performance in designs where the overall gain is >1 and the filter order is >2 over more typical high to low gain sequencing with increasing Q through the stages.

Benefits of Intersil's Stage Arrangements

Intersil's filter tool stage arrangements are designed to reduce the possibility of output clipping due to step response overshoot or frequency response peaking in each individual stage and lower the broadband integrated noise output from the filter. The reason is that high Q stages will always show a high spot noise peak in the frequency response and following these by lower Q or real pole stages will act to attenuate that peak relative to a design where the highest Q stage is the last stage [1].

An added benefit from the Intersil's sequencing is that amplifier bandwidth and slew rate requirements are clustered in a tighter range improving the probability of using a single op amp model type in a multi-stage design without excessive design margin in some of the stages. This again applies mainly when the overall filter gain >1. This helps the designer reduce cost and board space as many of Intersil's op amps are available in dual and quad versions.

Illustrative Example

Drawing from [2] an example of an 8th order Butterworth low pass filter with a gain of 100 and a cut off frequency of 100Hz will be executed. We will compare the output noise using the gain and Q sequence from [2] which is representative of typical practice against the strategy encoded into the Intersil filter design tool. It is important to note that the target cutoff frequency was increased from the 10Hz [2] to stay away from the 1/f noise region and we kept the relatively larger capacitor values used in [2]. However, we did let the active filter designer tool pick the resistor values (having set the cap values using the re-design feature of the tool) which lowered them to where only the op amp input voltage noise was making a meaningful contribution to the total output noise spectrum (14nV/$\sqrt{Hz}$ for the ISL28107 used in this example).

Following the stage arrangement more commonly used in the industry, the complete filter would have the following schematic as shown in Figure 1 with gain and Q sequencing from [2].

This arrangement is intended to reduce low frequency spot noise and running the high Q stages at unity gain reduces component sensitivity.
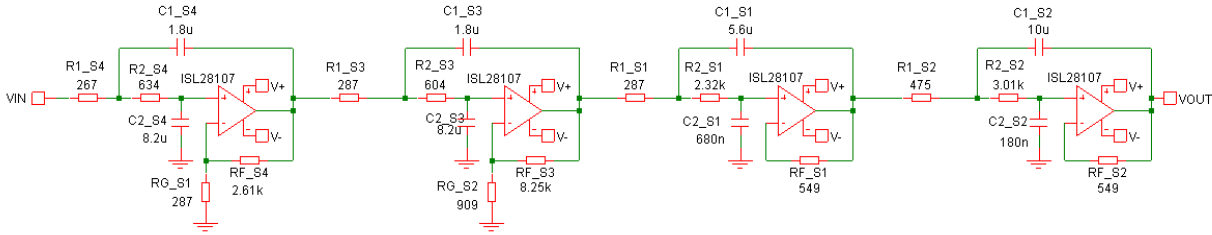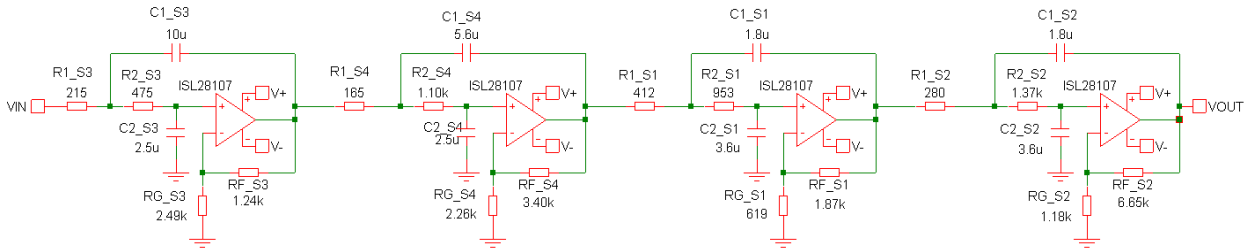
FIGURE 1. 8th ORDER BUTTERWORTH LOW PASS FILTER WITH TYPICAL GAIN AND Q SEQUENCING

TABLE 1. TYPICAL GAIN AND Q SEQUENCING

STAGE 1	STAGE 2	STAGE 3	STAGE 4
Gain: 10 V/V	Gain: 10 V/V	Gain: 1.0 V/V	Gain: 1.0 V/V
F_O: 100Hz	F_O: 100Hz	F_O: 100Hz	F_O: 100Hz
Q: 0.51	Q: 0.601	Q: 0.9	Q: 2.56

The Intersil active filter design tool supports up to 6th order filters. In order to implement this 8th order filter we manually designed the filter as two 4th order blocks then simulated in iSim PE. Following the sequencing strategy employed in the tool, and still forcing the C's to be so high as to push resistor values down to where they do not dominate the noise, we get the following test circuit shown in Figure 2. This gives the same gain and frequency response as [2] but with the gain spread between more stages.

FIGURE 2. 8TH ORDER BUTTERWORTH LOW PASS FILTER WITH INTERSIL GAIN AND Q SEQUENCING

TABLE 2. INTERSIL GAIN AND Q SEQUENCING

| STAGE 1	STAGE 2	STAGE 3	STAGE 4
Gain: 1.5 V/V	Gain: 2.5 V/V	Gain: 4.0 V/V	Gain: 6.67 V/V
F_O: 100Hz	F_O: 100Hz	F_O: 100Hz	F_O: 100Hz
Q: 2.56	Q: 0.9	Q: 0.601	Q: 0.51

To implement the filter we used the ISL28107 operational amplifier. A part that is similar to the devices used in [2].

The ISL28107 has low 1/f noise (<2Hz) and features very high open loop gain (50kV/mV) for excellent CMRR (145dB), and gain accuracy. This device is fabricated in a new precision 40V complementary bipolar DI process and its super-beta NPN input stage with bias current cancellation provides bipolar-like levels of AC performance with the low input bias currents approaching JFET levels [4].

The combination of low power (6.3mW on ±15V supply) and very high precision make this op amp a good choice to implement this 8th order high gain filter. The ISL28207 is the dual version of the ISL28107 and is available in an 8 Ld. SOIC package giving a lower cost and smaller board space path to implementation.

Simulation Results

We ran these simulations in iSim PE producing the spot output noise over frequency for each solution considered here. A critical aspect to accurate simulation is to have loaded the filter tool with improved and very accurate Pspice macromodels [3]. Both implementations give nearly identical frequency response shapes. A comparison zoomed in on the target F_{-3dB} frequency is shown in Figure 3.
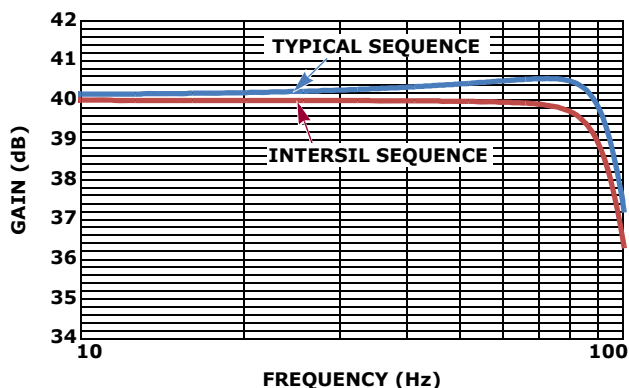
FIGURE 3. PASSBAND FREQUENCY RESPONSE COMPARISONS

The responses are not exactly identical - probably due to the 1% standard value snap on the resistors used in the filter design tool. They are, however, very close and nearly ideally flat with -3dB at 100Hz. These both continue on to show an 8-pole rolloff to >150dBc attenuation over the simulation frequency.

The output noise is, however, quite different between these two implementation alternatives. We would expect the 2nd circuit to show a bit higher low frequency output noise, but what is perhaps surprising is the high peak in the output noise given by the more typical gain and Q sequencing as shown in Figure 4.
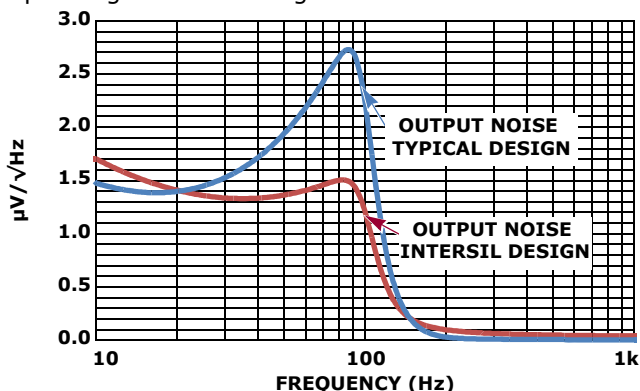

FIGURE 4. OUTPUT SPOT NOISE COMPARISON

The higher first stage gain of the first design following [2] does certainly give a slightly lower output noise at low frequencies (where Figure 4 is also showing a bit of 1/f noise corner effect that is included in the macro-model). But, because of the higher peaking in the later stages, that noise peaks up significantly more than the somewhat odd looking sequencing from the Intersil "Active Filter Designer". We would expect the first approach to integrate to a higher output noise V_{P-P} than the more rolled off approach of Figure 2.

Taking this spot noise plot and generating the output noise V_{P-P} that would be observed if a brick wall filter were swept from 10Hz to 1kHz, we get the plot in Figure 5. This is integrating to a V^2_{RMS} vs frequency then taking $6*V_{RMS}$ as an estimate of V_{P-P} noise. As expected from looking at Figure 4, the common approach of putting most of the gain early and the higher Q stages later gives a higher V_{P-P} noise. These both go flat at

higher frequencies as the spot noise rolls off (little additional noise power to integrate).
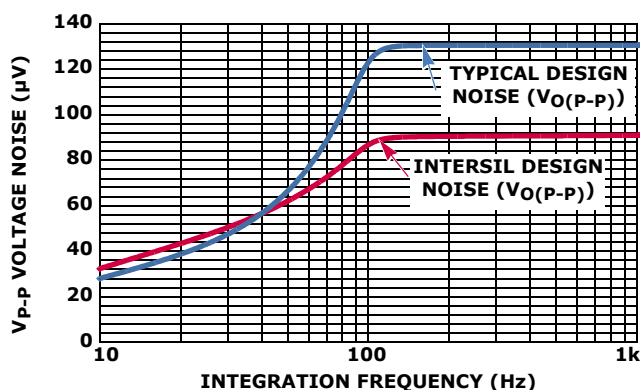

FIGURE 5. EXPECTED NOISE V_{P-P} ON OUTPUT

Assuming the noise measurement bandwidth after this stage is >200Hz, we would expect to see about 90µV$_{P-P}$ noise out of the ISL stage strategy vs 130µV$_{P-P}$ from a more typical approach. The "Active Filter Designer" algorithm seems to be moving in the right direction for integrated output noise but is somewhat counter-intuitive to long held ideas about multistage implementation strategies.

To look at the output clipping we introduced a ±100mV step at the input of the filter, this should produce a ±10V step on the output as we are trying to get the most of the ±15V supplies on the op amps. As this is a Butterworth filter, the step response will show some overshoot that increases with filter order. We expect that Intersil's arrangement will help reduce the interstage overshoot magnitudes limiting the possibility of clipping. A comparison of the step response is shown in Figure 6.
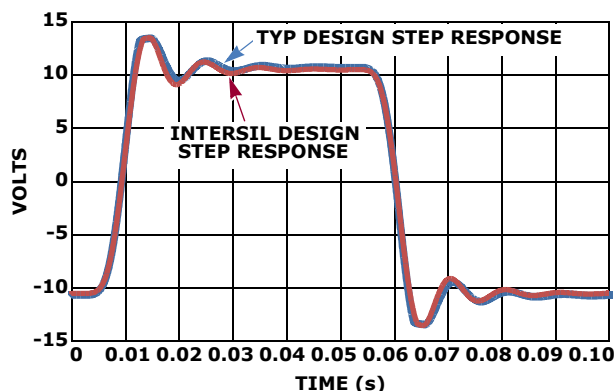
FIGURE 6. FILTER STEP RESPONSE

A closer look at the step response at the peak overshoot shows that the Intersil solution with reduced clipping while the more typical stage arrangement's step response is clipped due to the full final step response amplitude being applied to the highest Q stages.
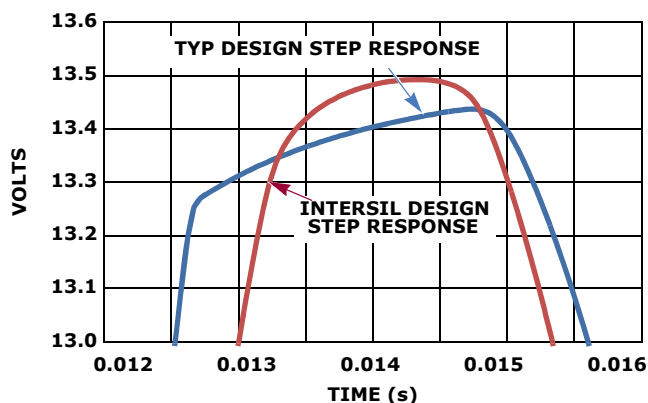
FIGURE 7. CLIPPING ON OUTPUT OF FILTERS

Summary

This example showed an improvement using the alternative approach encoded into the "Active Filter Designer". This becomes more dramatic for filter shapes requiring a larger spread in F_O and Q (like the 0.25dB Chebychev) and for higher cutoff frequencies. The exact gain settings chosen here may not be "optimized" for every factor to be considered in a multi-stage filter, but the general approach does seem to give a good compromise solution to a number of design considerations. The concern that lower gains in the first stage leads to higher output noise appears to be incorrect for either spot or integrated noise in this example. The filter tool is flexible enough to allow a designer to adjust the stage gains and Q sequencing to try alternate solutions. Porting test designs to iSim PE and transferring simulated noise data into Excel provides an easy path to further analysis and comparisons.

It is still true that combining high gain with high Q gives extreme Q sensitivity to gain accuracy. Here, a modest (but >1) gain is allocated to the highest Q stage. This is why the active filter designer does not also try to place a lot of the gain along with the highest Q in the schematics first stage. This relatively low gain in the first high Q stage helps reduce component sensitivity without degrading the total output noise - contrary to common assumptions.

If Q sensitivity to gain becomes a critical issue, using 0.5% resistors or going to gain of 1 in the highest Q first stage is recommended.

[1] Michael Steffes, Jian Wang, Oscar Mansilla. "Designer's Manual for the iSim Active Filter Designer" AN1548 Intersil Application Note http://www.intersil.com/data/an/an1548.pdf

[2] "8-Pole Active Low-Pass Filter Optimized for Precision, Low Noise, and High Gain Using the AD8622 and the ADA4062-2 Op Amps" CN-0127 Analog Devices Circuit Note

[3] Don LaFontaine, "Building an Accurate SPICE Model for Low Noise, Low Power Precision Amplifiers" AN1556 Intersil Application Note http://www.intersil.com/data/an/an1556.pdf

[4] ISL28107, ISL28207 FN6631 Intersil Datasheet http://www.intersil.com/data/fn/fn6631.pdf

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